Amendments to the Specification:

Please amend the Abstract of the Invention on page 43 as follows:

A multi-modulus divider for producing a low-noise divided output, wherein one embodiment comprises a low-noise frequency divider comprising a pulse-swallow configured divider module and first, second, and third latching blocks. The pulse-swallow configured divider module produces a pre-scaled divider output and a divided oscillation. The divided oscillation is sequentially latched by the latching blocks, wherein the divided oscillation and pre-scaled divider output, coupled as clocks to the latching blocks, resynchronize the divided oscillation to substantially eliminate noise. ~~An alternate embodiment includes a buffer operably coupled to the input of the low-noise frequency divider to reduce capacitive loading.~~ The first and second latching blocks are biased by a first bias signal and the third latching block is biased by a second bias signal wherein the second bias signal is larger than the first bias signal. Each latching block includes an output load device wherein the impedance of the third latching block is smaller than the impedance of the other output load devices. ~~An alternate embodiment comprises a plurality of dividers to produce the divided oscillation based on a modulus control signal.~~